

REMARKS

Claims 9-18 are pending. Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

I. REJECTION OF CLAIMS 9-18 UNDER 35 U.S.C. § 103(a)

Claims 9-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ouyang et al. (US publication 2004/0256639) in combination with Lin et al. (US publication 2005/0035369), Yeo et al. (US publication 2005/009263), Chidambarrao et al. (US publication 2005/0164477), and Currie et al. (US publication 2004/0173812). Withdrawal of the rejection is respectfully requested for at least the following reasons.

- i. Ouyang et al. do not teach a PMOS device with source, drain and channel regions formed within the substrate, as recited in claim 9, and no motivation exists for a modification thereof.*

Claim 9 is directed to a method of fabricating a semiconductor device, and comprises forming a PMOS device. The PMOS device has ***source, drain and channel regions formed within the substrate***. Ouyang et al. do not teach this feature. Rather, the cited reference teaches a PMOS device that is ***vertically oriented***, wherein the source and channel region are ***not formed within the substrate***.

More particularly, Ouyang et al. disclose a vertical channel PMOS device in Figs. 5-7, and corresponding text. The PMOS device comprises a mesa or vertical column 5000 that includes the source region 164 and the channel region 165 residing therein ***above*** the substrate. (See, e.g., [0030]). Clearly then, the reference does not teach or suggest the invention of claim 9.

Not only does the cited reference not teach the invention, but no suggestion exists that would motivate one of ordinary skill in the art to modify Ouyang et al. in accordance with the claimed invention. Rather, ***the teaching within Ouyang et al.***

would tend to discourage such a modification to form the source, drain and channel regions within the substrate in a planar fashion as claimed. More particularly, the Background of Ouyang et al. discourages planar devices by stating that the channel length of planar devices is disadvantageously limited by lithography, as opposed to vertical type structures. (See, e.g., paragraph [0007]). Further still, in the Summary of Ouyang et al., **the reference indicates that it is not practical to integrate a nMOSFET on a (100) plane and a pMOSFET on a (110) plane using conventional silicon technology wherein source, drain and channel regions are within the substrate as claimed,** but it is easy to do so with vertical devices. (See, e.g., [0015]). Therefore one of ordinary skill in the art, upon evaluating the teachings of Ouyang et al., and the negative statements made therein regarding planar devices, would not have been motivated to modify Ouyang et al. in accordance with the present invention.

No other teaching associated with the other cited prior art references have been discussed in the Office Action in conjunction with the rejection of claim 9. However, after a review of the additional cited art, no teaching is found therein that would remedy the deficiencies in Ouyang et al. or overcome the negative teachings therein that discourage a modification thereof in accordance with applicant's claims. Therefore claim 9 and its associated depending claims is non-obvious over the cited art, and withdrawal of the rejection is respectfully requested.

II. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

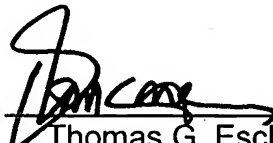


Serial No. 10/785,648
Page 7

Authorization is hereby given to the Commissioner to charge any other fees due as a result of the filing of this response to Deposit Account Number 20-0668, TI-36595.

Respectfully submitted,
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: December 20, 2006


Christine Gillroy